REMARKS

Claims 9-21 and 46 are pending in this application. Claim 13 has been amended. No new matter has been introduced. Applicant acknowledges with appreciation the indication in the April 13, 2006 Office Action that claims 9-12 and 46 are allowed.

Claims 13-15 and 17-19 stand rejected under 35 U.S.C. §102(b) as being anticipated by Blair et al. (U.S. Patent No. 6,171,901) ("Blair"). This rejection is respectfully traversed.

The claimed invention relates to a method of forming a memory cell. As such, amended independent claim 13 recites a "method of forming a memory cell" by *inter alia* "forming a transistor including a gate fabricated on a semiconductor substrate, said step of forming said transistor including providing a silicide region of said gate." Amended independent claim 13 also recites "forming a capacitor adjacent said transistor by providing a first conductive layer, a dielectric layer and a second conductive layer." Amended independent claim 13 further recites that "said steps of providing said first conductive layer, said dielectric layer and said second conductive layer are conducted prior to said step of providing said silicide region of said gate." Amended independent claim 13 additionally recites "forming source/drain regions in said semiconductor substrate disposed adjacent to said gate, said step of forming said source/drain regions being conducted subsequent to said step of forming said silicide region of said gate."

Blair relates to a "process flow for forming a polysilicon-to-polysilicon capacitor" that "performs the capacitor anneal step in a nitrous oxide ambient." (Abstract). Blair teaches that "a nitroxide layer forms over heavily doped polysilicon of the upper electrode of the capacitor" and that "[T]his nitroxide layer acts as a barrier

against the diffusion of oxygen, preventing further oxidation of the heavily doped polysilicon electrode layer during the subsequent seal oxidation step." (Abstract). Blair also teaches that the nitroxide barrier layer "is readily removed along with the other seal oxide layers immediately before formation of the silicided capacitor electrode contacts." (Abstract).

Blair fails to anticipate the subject matter of claims 13-15 and 17-19. Blair does not disclose, teach or suggest "forming a transistor including a gate fabricated on a semiconductor substrate, said step of forming said transistor including providing a silicide region of said gate" and "forming source/drain regions in said semiconductor substrate . . . subsequent to said step of forming said silicide region of said gate," as claim 13 recites. Blair teaches that source/drains 340 of CMOS device 342 are first formed by implantation with a source/drain mask 338, and that only then seal oxide layers 344a and 344b and silicide contacts 344 are formed over the upper and lower capacitor electrodes. (Col. 5, lines 48-51; col. 6, lines 1-9). Thus, Blair does not disclose "forming source/drain regions in said semiconductor substrate . . . subsequent to said step of forming said silicide region of said gate," as recited in amended independent claim 13. For at least the reasons above, the subject matter of claims 13-15 and 17-19 is not anticipated by Blair, and withdrawal of the rejection of these claims is respectfully requested.

Claim 16 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Blair. Claims 20 and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Blair in view of Crafts (U.S. Patent No. 5,973,952) ("Blair"). These rejections are respectfully traversed.

Claim 16 depends on amended independent claim 13 and recites that the second conductive layer "is formed by deposition at a temperature between about

600ºC to about 800ºC." Claims 20 and 21 also depend on amended independent claim 13 and recite that the memory cell is "a DRAM" (claim 20) and "one of a DRAM, flash memory or SRAM" (claim 21).

Crafts relates to a "shielding conductor . . . spaced from a matrix of memory cells in a dynamic random access memory (DRAM) to shield the memory cells from noise signals, such as the noise created by components of a system level integrated circuit (SLIC)." (Abstract). Crafts teaches that the shielding conductor "is connected to one of a reference or potential source, preferably external to the DRAM segment" and that it "distributes the effect of noise and maintains a uniform reference potential with respect to the DRAM components with which it overlays or connects." (Abstract).

The subject matter of claim 16 would not have been obvious over Blair, and the subject matter of claims 20 and 21 would not have been obvious over Blair and Crafts, whether considered alone or in combination. Specifically, the Office Action fails to establish a *prima facie* case of obviousness. Courts have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573 (Fed. Cir. 1996).

In the present case, Blair and Crafts, alone or in combination, do not disclose, teach or suggest all limitations of claims 16, 20 and 21. As noted above, Blair does not disclose "forming a transistor including a gate," "providing a silicide region of said gate" and "forming source/drain regions in said semiconductor substrate . . .

subsequent to said step of forming said silicide region of said gate," as claim 13 recites. Crafts does not rectify the deficiencies of Blair. Crafts teaches an embedded DRAM with a noise protection shielding conductor, and not the step of "providing a silicide region of said gate," much less the steps of "providing said first conductive layer, said dielectric layer and said second conductive layer . . . prior to said step of providing said silicide region of said gate" and "forming source/drain regions in said semiconductor substrate . . . subsequent to said step of forming said silicide region of said gate," as in the claimed invention. For at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness and withdrawal of the rejection of claims 16, 20 and 21 is respectfully requested.

Allowance of the application is solicited.

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Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
Gabriela I. Coman
Registration No.: 50,515
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant